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09/647,431	10/02/2000	Andreas Klug	112740-112	8643

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EXAMINER	
MILLS, DONALD L	
ART UNIT	PAPER NUMBER
2662	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/647,431	KLUG, ANDREAS	
	Examiner	Art Unit	
	Donald L Mills	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 11 and 20 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 11 and 20, the claim specifies *a control signal sequence*, therefore, the term *control signals* lacks proper antecedent basis. Furthermore, the relationship between the control signals and the control signal sequence is not clear from the context of the claim. For the purpose of this examination, the examiner will interpret *control signals* as *the control signal sequence.*

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 11, 12, and 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada et al (US 5,412,655), hereinafter referred to as Yamada.

Regarding claims 11 and 20, Yamada discloses a system, which comprises:

Generating (Claim 11)/A generator for generating (Claim 20) a control signal sequence with a clock rate corresponding to the overall payload cell rate C_{RN} of the N time-division multiplex communication terminals, whereby the control signals represent one of a first and a second status (Referring to Figure 1, cell disassembly control unit 2 controls the buffer memory, inherently comprising a clock rate that is compatible with the TDM data highway **11** and controls the transmission of cells or idle traffic. See column 5, lines 54-59.)

Offering (Claim 11)/A device for offering (Claim 20) a fixed data pattern (Referring to Figure 2, the idle data transmission controller **204** generates idle data. See column 6, line 21.)

Transmitting (Claim 11)/A first transmitter for transmitting (Claim 20) ATM cells coming from the ATM communication layer into an ATM cell waiting list (Referring to Figure 1, transmitted cells from the ATM highway **5** is stored into buffer memory **12**. See column 5, lines 12-14.)

Transmitting, on demand, (Claim 11)/A second transmitter for transmitting (Claim 20) an ATM cell from the ATM waiting list to the requesting time-division multiplex communication terminal when a respectively oldest control signal of the control signal sequence represents the first status (Referring to Figure 2, a cell, stored in buffer memory **12**, is transmitted to the TDM data highway **11**, when the cell disassembly control unit **2** detects a cell. See column 6, lines 22-28,) *and transmitting the fixed data pattern to the requesting time-division multiplex communication terminal when the oldest control signal of the control signal sequence represents the second status* (Referring to Figure 2, idle data is outputted to TDM data highway **11** when the cell disassembly control unit **2** does not detect a cell. See column 6, lines 28-30.)

Deleting (Claim 11)/A device for deleting the oldest control signal of the control signal sequence (Referring to Figure 2, by definition signals generated by the cell disassembly control unit **2** for controlling the reading of data from the buffer memory are automatically deleted after transmission.)

Regarding claim 12, Yamada discloses:

Allocating a control signal that represents the first status to each ATM cell of the ATM waiting list in the control signal sequence (Referring to Figure 2, when the cell disassembly control unit **2** detects a cell stored in buffer memory **12** it is transmitted. See column 6, lines 22-28.)

Carrying out a check, when a new control signal of the control signal sequence is generated in coincidence with the prescribed clock rate to see whether an ATM cell to which no control signal representing the first status is allocated is still present in the ATM waiting list (Referring to Figure 2, carrying out a check is inherently performed when the cell disassembly control unit **2** detects a cell stored in buffer memory **12** before transmission can begin. See column 6, lines 22-28.)

Generating a control signal representing the first status when an ATM cell to which no control signal representing the first status is allocated is still present in the ATM waiting list; and (Referring to Figure 2, when the cell disassembly control unit **2** detects a cell stored in buffer memory **12** it is transmitted. See column 6, lines 22-28.)

Generating a control signal representing the second status when an ATM cell to which no control signal representing the first status is allocated is not present in the ATM waiting list

(Referring to Figure 2, when the cell disassembly control unit **2** does not detect a cell idle data is outputted to TDM data highway **11**. See column 6, lines 28-30.)

Regarding claims 15, 16, and 17, Yamada discloses *the method further comprising the step of enabling a cell transmission from the ATM communication layer into the ATM waiting list when the plurality of ATM cells present in the waiting list minus the plurality of control signals of the control signal sequence representing the first status is ≤X (Claim 15)/wherein X ≥ 1 (Claim 16)/wherein X = 1 (Claim 17)* (Referring to Figure 2, the cell accumulation controller **1** writes the payload data of the cell, each time an ATM cell is received, on the unused bank of the buffer memory **12**, which is inherently performed when the control signal is issued because it is the difference between the number of ATM cells present in the buffer minus the control signal, which is always greater than or equal to an arbitrary number including the number one. See column 6, lines 4-6.)

Regarding claim 18, Yamada discloses *wherein the N time-division multiplex terminals are uncorrelated* (Referring to Figure 2, a cell or idle data is transmitted to the TDM data highway **11**, which inherently is uncorrelated because there is only one TDM data highway **11**. See column 6, lines 22-28.)

Regarding claim 19, Yamada discloses *the method further comprising the step of dividing the ATM cells and the cells containing the fixed data pattern onto the N communication terminals according to a round-robin method* (Referring to Figure 2, a cell or idle data is transmitted to the TDM data highway **11**, which by definition acts as the round-robin method since when cell or idle data is serviced at one time. See column 6, lines 22-28.)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (US 5,412,655), hereinafter referred to as Yamada.

Regarding claim 13 as stated above in the rejection statement of claim 11, Yamada discloses all the claim limitations of claim 11 (parent claim). Yamada does not disclose *wherein the control signal representing the first status is represented by a logical "1" and the control signal representing the second status is represented by a logical "0".*

Yamada teaches a multiprocessing system for ATM cells, which comprises transmitting a cell from buffer memory **12** when a cell is detected by cell disassembly control unit **2** and sending idle traffic when the cell disassembly control unit **2** does not detect a cell (See column 6, lines 22-30.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to manipulate the signal generated by the cell disassembly control unit **2** as a logical "1" when a cell is detected and a logical "0" when a cell is not detected. One of ordinary skill in the art would have been motivated to so in order to make a clear distinction between the control signals.

Regarding claim 14 as stated above in the rejection statement of claim 11, Yamada discloses all the claim limitations of claim 11 (parent claim). Yamada does not disclose *wherein the control signal sequence has a length of up to 3•N signals.*

Yamada teaches a multiprocessing system for ATM cells, which comprises transmitting a cell from buffer memory **12** when a cell is detected by cell disassembly control unit **2** and sending idle traffic when the cell disassembly control unit **2** does not detect a cell (See column 6, lines 22-30.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to manipulate the variable length of the signal generated by the cell disassembly control unit **2** as a signal with length 3•N. One of ordinary skill in the art would have been motivated to so because increasing the length of the control signal would provide increased error correction.

Response to Arguments

7. Applicant's arguments filed February 19, 2004 have been fully considered but they are not persuasive.

Rejection Under 35 USC § 112

Applicant fails to address Examiner's 112 2nd paragraph rejection. Regarding claims 11 and 20, for the purpose of this examination, the examiner interpreted *control signals* as *the control signal sequence* because the relationship between the control signals and the control signal sequence is unclear from the context of the claim.

Rejection Under 35 USC § 102

On page 3 of the remarks, regarding claims 11 and 20, Applicant argues that Yamada does not disclose "a control signal sequence having a clock rate corresponding to the overall payload cell rate CR_N of N time-division multiplex communication terminals" and "transmitting ATM cells from an ATM cell waiting list when a respective oldest control signal of the control signal sequence represents a first status, transmitting a fixed data pattern when the respective oldest control signal of the control signal sequence represents a second status, then deleting the oldest control signal of the control signal sequence." Examiner respectfully disagrees.

Yamada discloses a cell disassembly control unit 2, which controls the buffer memory, inherently comprising a clock rate that is compatible with the TDM data highway **11** and controls the transmission of cells or idle traffic corresponding to the overall cell rate of the nodes that transmit the TDM data (See column 5, lines 54-59.) Therefore, Yamada anticipates "a control signal sequence having a clock rate corresponding to the overall payload cell rate CR_N of N time-division multiplex communication terminals."

Yamada discloses transmitting, a cell stored in buffer memory **12**, to the TDM data highway **11** when the cell disassembly control unit **2** detects a cell (See column 6, lines 22-28.) And, idle data is transmitted to the TDM data highway **11** when the cell disassembly control unit **2** does not detect a cell (See column 6, lines 28-30.) The examiner interprets the control signal generated by the cell disassembly unit **2**, inherently representing a status for each transmission, as the "oldest control signal sequence." By definition, signals generated by the cell disassembly control unit **2** for controlling the reading of data from the buffer memory are automatically terminated after transmission. Therefore, Yamada anticipates "transmitting ATM cells from an ATM cell waiting list when a respective oldest control signal of the control signal sequence

represents a first status, transmitting a fixed data pattern when the respective oldest control signal of the control signal sequence represents a second status, then deleting the oldest control signal of the control signal sequence."

Rejection Under 35 USC § 103

On page 4 of the remarks, regarding claims 13 and 14, Applicant argues that Yamada does not disclose "a control signal sequence having a clock rate corresponding to the overall payload cell rate CR_N of N time-division multiplex communication terminals" and "transmitting ATM cells from an ATM cell waiting list when a respective oldest control signal of the control signal sequence represents a first status, transmitting a fixed data pattern when the respective oldest control signal of the control signal sequence represents a second status, then deleting the oldest control signal of the control signal sequence." Examiner respectfully disagrees. See comments above for the corresponding arguments.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donald L Mills whose telephone number is 703-305-7869. The examiner can normally be reached on 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 703-305-4744. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donald L Mills
DLM
April 12, 2004

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